## Explanations for the Trigger selections in AIDA

The Trigger selections , shown below, are made in the Local Controls window of the AIDA browser.

| Trigger Selection table ( Version 8 ) | Signal names are from VHDL |
|---|---|
| 0 : ASIC1_Data_Ready | 8: ASIC1_OR_16 |
| 1 : ASIC1_rdo_range AND ASIC1_Data_Ready | 9: ASIC2_OR_16 |
| 2 : ASIC2_rdo_range AND ASIC2_Data_Ready | 10: ASIC3_OR_16 |
| 3 : Led_Trigger(0) | 11: ASIC4_OR_16 |
| 4 : OR64 | 12: OR of all OR16s |
| 5 : Readout_Done(0) | 13: Led_Trigger(1) |
| 6 : Sync_registered | 14: Logic 0 |
| 7 : Force_capture | 15: Readout_Done(1) |

*Selection 4* : OR64 is the logic OR of the masked discriminator signals from the ASICs. The masks are setup using the Discriminator Controls window. The FPGA is programmed to produce a 10ns pulse when an unmasked discriminator input from the ASIC goes from false to true.

*Selections 8 to 11* are the OR16 signals from the ASICs and are not subject to the masks. It should be noted that the ASIC OR16 signals will have a widely varying pulse width.

*Selection 12* is the OR of all the OR16 signals from the ASICs.

*Selection 6* is the registered SYNC pulse as it is received in the FEE64 from the MACB via the HDMI cable. It can be used to diagnose problems with the SYNC distribution.

*Selection 3 and 13* are the signals from the VHDL Leading Edge Discriminator for channel 0 and 1 of ASIC 0.

*Selection 14*, Logic '0', should be used if the FEE64 is not intended to contribute to the final Trigger output from the base level MACB.

*Selections 0,1,2,5,7,15* are really for use in debugging the VHDL.