Specification for the multiplicity Trigger for AIDA

In the FPGA VHDL the following logic will be implemented to create a Multiplicity Window Trigger.

>   A discriminator signal is true if the input is over the ASIC threshold (internal to the ASIC).
>   A discriminator signal can be masked before use by the Trigger Logic (at the FPGA input).
>   Every 10nS:-
>   Calculate the number of the 64 discriminator signals that are true. (N)
>   If N =< 'Upper Limit' AND N >= 'Lower limit' for more than a specified number (T)of

clock cycles then

>   Trigger is true
>   Else
>   Trigger is false
>   End if

This will produce a Trigger pulse with a minimum width of 10ns and a maximum depending on how long the logic remains true.

Controls in the Discriminator browser window are :-
>   Upper Limit   0 to 64
>   Lower Limit   0 to 64
>   Number clocks (T) to be stable   4 to 60 in steps of 4.

The Trigger will be selected to be output from the FEE64 on the Trigger signal by selection 5 in the Trigger O/P control register in the Local Controls Browser window.

Readout_Done(0) signal will be removed from the choices available.