A modular amplifier system for the readout of silicon strip detectors

S.L. Thomas
Rutherford Appleton Laboratory,
Chilton, Didcot, OXON, OX11 0QX, UK

T. Davinson , A.C. Shotter
Department of Physics, University of Edinburgh,
Edinburgh, EH9 3JZ, UK

Abstract

A modular system of 250 pre-amplifiers and shaping amplifiers is being built to read out an array of silicon strip detectors . The detectors form a telescope which is used to study the break up reactions of heavy ions in vacuum. A charge sensitive pre-amplifier connected to each strip amplifies the signal before it is passed to the second stage of amplification and shaping. An ADC converts the final signal to digital form before processing by a computer, where information on particle identity, scattering direction and energy is extracted.

The pre-amplifiers have been designed as thick-film hybrids in order to achieve the high circuit density required in the vacuum chamber. The hybrids plug into a mother-board from which twisted-pair cables carry the signals to the shaping amplifiers outside the chamber.

The shaping amplifiers are surface-mounted boards, plugged into a Eurocard to which the cables are attached. The amplifiers feature three stages of shaping and a gain which can be adjusted by changing resistor packages on the Eurocard. The linearity of the amplifiers is better than 0.1% for outputs up to 10V, with a peaking time of $1\mu s$. The output noise is below 1.0 mV rms at maximum gain, equivalent to 500 electrons rms in the detector.

1 Introduction

The use of silicon strip detectors (SSDs) in particle physics experiments is now well established. In many of these experiments, the beam interactions occur at a known time and a switched amplifier system can be used in the detector readout. Such a system can be easily integrated such that a large number of channels can be instrumented. The present work is concerned with electronics for the readout of SSDs in the application of nuclear structure physics, where interactions occur continuously in time. In this case a preamplifier and shaping amplifier are required for each channel, instead of gated integration. Currently, amplifier modules are used, but the high cost limits the number of strips that can be read out. There is a need for a low cost alternative which will allow the advantages of SSDs to be exploited in the field of nuclear physics, as in particle physics. The Rutherford Appleton Laboratory is building such a system in collaboration with the Nuclear Physics group at Edinburgh University (Reference 1).

A block diagram of this modular system is shown in Figure 1. The Charge Sensitive Pre-Amplifiers (CSPAs) are mounted in motherboards as close as possible to the SSDs in the vacuum chamber. Ribbon cables connect the CSPA motherboards to shaping amplifiers (SAs) outside the chamber. A discriminator on each SA board generates a trigger pulse when a signal above a certain threshold is received from the CSPA. A separate logic board then determines whether a valid event has occurred so that peak-sensing ADCs can be triggered.

The major constraints on the design of the system have been the needs for low cost high-density circuitry. The specification of the system is close to that of commercial modules and is shown in detail in Tables 1 and 2. It has been necessary to sacrifice some flexibility to achieve the low cost though many parameters can still be adjusted. The SAs have trimmers to adjust the pole-zero cancellation and to set the output voltage to zero. The gain of the SAs and the width of discriminator outputs are controlled by resistors which plug into the motherboard. A single trim-pot on the motherboard set the threshold voltage for all SAs on the board.

2 Design of CSPA

In order to reduce the distance to the SSDs, the CSPAs need to be mounted inside the vacuum chamber. The high circuit density required in the vacuum meant that the circuitry had to be realised as a thick-film hybrid. Each CSPA is built on a separate substrate and is packaged in a 12 pin single-in-line (SIL) format. The hybrids plug upright into sockets in mother-boards which are themselves connected to the SSDs by a short length of ribbon cable. There are 32 CSPA channels per board, corresponding to one channel per strip. Twisted pair cable connects the hybrid outputs to the shaping amplifiers located outside the vacuum chamber.

Two versions of the CSPA have been developed in order to amplify both positive and negative signals. This allows the pre-amps to be used with double-sided SSDs. The only difference between the circuits lies in the output stage, as shown in Figures 2a and 2b. The gain stage common to both designs employs an FET and two bipolar transistors in a cascode configuration, to give an open loop gain of around 2500. The FET is biased at $g_m = 16mS$ for which its input noise is $0.85nV/\sqrt{Hz}$ (Reference 2). In circuit (a) the amplified signal is buffered by an NPN darlington stage, whereas circuit (b) uses a PNP output stage. The gain of both circuits is determined by the value of the feedback capacitor, which with the feedback resistor also determines the decay time. Low pass filters have also been incorporated in order to increase the rejection of high frequency power supply noise. The circuits have an output resistance of 100Ω, equal to the impedance of the twisted pair cable, and drive into 100Ω at the shaping amplifier input. The signal is therefore attenuated by a factor of two. AC coupling through $10\mu F$ reduces the static current in the hybrid,as the output voltage is not exactly at ground potential.

Although the hybrid thick film layouts differ, the pinouts of the two circuits are similar. This simplifies the layout of the board on which the pre-amps are mounted (Figure 3). In each design all 8 ground pins are connected together by the earth plane which covers the reverse face of the substrate. Using the earth plane improves the circuit grounding, but also helps transport the heat generated by the circuitry off the hybrid. In order to minimise the physical size of the hybrids, the main power supply decoupling components are

left off the substrate and instead positioned on the mother-board.

3 Design of SA and Discriminator

The SAs have been designed as surface mounted boards, again to achieve high density. Eight SAs plug horizontally into a double height Eurocard to which are connected input and output twisted pair cables (Figure 4). Resistor packs plug into the mother-board and control the gain of the SAs and the width of the discriminator outputs. Up to 16 Eurocards are mounted in a 19" sub-rack, giving 128 channels in total.

Each SA board contains a differential input buffer (NE5539) followed by four stages of amplification with shaping (Figure 5). The discriminator takes its input from the buffer output which retains the fast rising edge from the CSPA. The C-R differentiation has a time constant of 200ns, so the output of the comparator (SP9685) is a pulse of width >200ns, provided the threshold voltage is sufficiently low. The pulse is then shortened by a circuit on the mother-board, which allows the pulse width to be adjusted from 30-200ns. The threshold voltage can be set to a minimum of around 4mV, for which signals of peak height 10mV will produce full width (200ns) pulses. (At lower thresholds, oscillations tend to occur as the comparator approaches its linear region). The minimum threshold is equivalent to a particle energy of 1 MeV if the input buffer is unity gain, or 0.1MeV for a gain of 10.

The first stage of shaping follows the pole-zero cancellation circuit which removes the slow $50\mu s$ decay of the CSPA output. The LM318 has unity gain and contributes a input-referred noise of about $15nV/\sqrt{Hz}$. The second stage of shaping is an OP37 at a gain of 3.1 which is followed by an amplification stage (OP37 with a gain of 3.3). The buffered signal then drives a Robinson base-line restoration circuit (Reference 3), which is set at a current level of 0.15mA. The restoration rate is given by

$$\frac{dV}{dT} = \frac{i}{C} = \frac{0.15 \times 10^{-3}}{100 \times 10^{-9}} = 1.5mV/\mu s$$

This rate is low enough to maintain the high linearity of the amplifier, but is sufficient to eliminate baseline shift at rates up to 10kHz.

The final stage of amplification is an LM318 (gain 1.7) which has the high slew rate ($> 70V/\mu s$) necessary to drive the fast 10V output.

4 Summary of design calculations

4.1 CSPA noise analysis

The CSPA noise is specified in terms of energy measured at the output of the SA. The effect of shaping is therefore taken into account. A convenient method of analysis is to use noise weighting functions (Reference 4). The transfer function of the CSPA and SA together is

$$H(s) = \frac{G\tau}{2C_f(1+s\tau)^3}$$

where G is a gain constant, with an impulse response

$$h(t) = \frac{Gt^2e^{(-t/\tau)}}{4C_f\tau^2}$$

$h(t)$ reaches the peak of $G/(e^2C_f)$ at $t = 2\tau$ where τ is the shaping time constant ($0.5\mu s$). The normalised response is therefore

$$w(t) = \frac{t^2e^{(2-t/\tau)}}{4\tau^2}$$

The equivalent noise charges at input are then given by

$$ENC_s^2 = 0.5e_n^2(C_{in}+C_d)^2\int_{-\infty}^{+\infty}[w'(t)]^2dt$$

and

$$ENC_p^2 = 0.5i_n^2\int_{-\infty}^{+\infty}[w(t)]^2dt$$

where

$$e_n^2 = 4kT\left(\frac{0.7}{g_m}+\frac{1}{R_Lg_m^2}\right)$$

and

$$i_n^2 = 4kT/R_f$$

Substituting $g_m = 0.016$, $R_L = 390\Omega$, $R_f = 22.7M\Omega$, $C_d = 0$pF and $C_{in} \approx C_{FET} \approx 20$pF we obtain $e_n = 0.94nV/\sqrt{Hz}$ and $i_n = 27fA/\sqrt{Hz}$. The noise weighting integrals are $0.853/\tau$ (series) and

2.56τ (parallel) so the equivalent noises are $ENC_s = 108$ electrons and $ENC_p = 130$ electrons.If the $22M\Omega$ detector bias resistor is included,a further 130 electrons noise is generated, and the total is 215 electrons rms. The noise slope is 5.5 electrons/pF.

4.2 Calculation of SA gain

The gain of the shaping and amplification stages must be chosen such that at maximum gain a 0.4V (20MeV) pulse from the CSPA produces a 10V output, ie a gain of 25. From section 4.1 we know that the system impulse response peaks at $G/(e^2C_f)$.The impulse response of the CSPA alone has a peak $1/C_f$, so the ratio of SA output to CSPA output is G/e^2 Therefore we require $G/e^2 = 25$ or $G = 185$. The NE5539 gain must be set as high as possible in order to maximise the input to the discriminator. The output of the NE5539 is limited to about 2.2V, so the highest gain for a 0.2V input will be 10.The gain of the subsequent shaping and gain stages must therefore be 18.5 .

4.3 SA noise analysis

The noise at the output of the SA must be below 1.0mV rms so the choice of the op-amps and gains of successive stages is critical. The op-amps must also have a high slew-rate in order to reduce non-linearity for large signals. Two op-amps were considered for this design, namely the OP37 and the LM318. The latter device is faster (up to $120V/\mu$s for rising edges) but is considerably noisier than the OP37. The total output noise due to the first op-amp stage is given by

$$e_{out}^2 = 0.5e_n^2 \int_{-\infty}^{+\infty} [h(t)]^2 dt$$

where

$$h(t) = \frac{Gte^{-t/\tau}}{\tau^2}$$

and e_n is the op-amp rms input noise density. Evaluating the integral we obtain $e_{out} = e_n \times 10^4$. If the first stage is an LM318, its contribution to the output noise is 0.15mV rms which is well within the specification of 1.0mV rms. The LM318 is preferable to the OP37 for the first shaping stage because of the fast rising edges from the NE5539 which could cause an OP37 to slew-limit. The

second and third stages use the OP37 for low noise, but the output stage again requires the faster slew rate of the LM318. (The maximum slew rate at output is $17V/\mu s$ which is close to the limit for the OP37). A SPICE analysis of the whole circuit predicts that the noise from the other op-amps and resistors will increase the total noise to about 0.47mV rms. In Figure 6, the simulated output noise spectrum shows the relative contributions of the most significant noise sources.

5 Performance of prototype system

5.1 CSPA noise measurements

The pre-amp noise has been plotted against added capacitance C_d in Figure 7. The noise was measured at the CSPA output with a wide-band power meter and the noise density evaluated by dividing the power by the noise bandwidth ($\pi/2$ times the upper 3dB frequency).

The graph shows a linear relationship between noise and C_d, with a gradient of $0.5nV/\sqrt{Hz}/pF$. We expect the output noise density to be given by

$$e_{out} = e_n \left(1 + \frac{C_d + C_{in}}{C_f}\right)$$

so the noise gradient is

$$\frac{\partial e_{out}}{\partial C_d} = \frac{e_n}{C_f}$$

Therefore

$$e_n = 0.5 \times 2.2 = 1.1nV/\sqrt{Hz}$$

This value is close to the expected value of $0.94nV/\sqrt{Hz}$ obtained in section (4.1) . The measured noise performance is equivalent to about 160 electrons rms at $C_d = 0$, with a noise slope of 6.3 electrons/pF.The measurements were made without the detector bias resistor, which would increase the noise to 205 electrons. This value is well below the specification of 330 electrons, but it must be remembered that the CSPA motherboard may increase the capacitance on the input by a few pF, increasing the noise slightly.

5.2 SA noise measurements

The SA noise was measured with a spectrum analyser and is shown in figure 8. The curve shows the expected roll-off in noise (owing to the shaping) with a value at 10kHz of -10dB$\mu V/\sqrt{Hz}$ or $0.30\mu V/\sqrt{Hz}$. This is in good agreement with the simulation of Figure 6. The measured noise is higher than predicted for frequencies above about 1MHz, however.

This discrepancy was confirmed by a measurement with a wide-band power meter, which showed that the total noise was 0.7mV rms, higher than the expected value of 0.47mV rms. This is still within the original specification of 1.0mV, so the performance is acceptable. One reason for the discrepancy is that there is slight gain peaking in the OP37 stages, which are operating below their optimum gain of 5. This effect was not modelled by the SPICE simulation.

5.3 Linearity measurements

Both the CSPA and SA are required to be linear to better than 0.1%. Measurements have been made with a multi-channel analyser and a precision pulse generator which confirm that both circuits are well within the specification. Typically, the linearity was of the order of 0.03%, which is at the limit of resolution of the measurement apparatus.

6 Conclusions

It has been demonstrated that a low-cost modular amplifier system can adequately meet the specifications for instrumentation in Nuclear Structure Physics. Measurements on a prototype system of 32 channels have confirmed that the circuits are behaving in accordance with design calculations. The full system of 256 channels will be completed after beam tests on the prototype.

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of the CSPA, J C Stanton for initial design work on the SA and P Jobanputra for his work on the layout of the SA board.

References

(1) T. Davinson,A.C. Shotter, P. Jobanputra, A.J. Stephens, S.L. Thomas.Development of a Silicon Strip Detector Array for Nuclear Structure Physics. To be published in NIM.

(2) E. Gatti,P. F. Manfredi.Nuovo Cimento Vol 9, Series 3, Number 1 (1986) 112

(3) P. W. Nicholson.Nuclear Electronics p113. Wiley Interscience (1974)

(4) V Radeka. IEEE Trans on Nuclear Science NS-21 (1974) 51

Figure captions

(1) Block diagram of amplifier system

(2a) Charge sensitive pre-amplifier (positive output)

(2b) Charge sensitive pre-amplifier (negative output)

(3) CSPA mother-board (32 channels)

(4) SA mother-board (8 channels)

(5) Shaping amplifier and discriminator circuit

(6) Simulated shaping amplifier noise spectrum

(7) Variation of CSPA output noise density with detector capacitance

(8) Measured noise spectrum at output of SA

Sensitivity	**20mV/Mev or 73nV/electron**
Noise[1]	**<3keV FWHM (330 electrons rms) at 0pF**
Noise slope	**<90eV/pF (10 electrons/pF)**
Input capacitance	**0-300pF**
Rise time (10-90%)	**<20ns (C_d =0pF), <40ns (C_d =100pF)**
Fall time (0-63%)	**50μs**
Dynamic range[2]	**0-200 MeV ($\pm$ 4V)**
Integral non-linearity	**<0.1%**
Output impedance	**100Ω (AC coupled)**

[1] The effect of shaping is taken into account
[2] There are two versions of CSPA, one for positive, the other for negative outputs.

Table 1: Charge-sensitive Pre-amplifier specification

Shaping	**$CR-(RC)^2$**
Shaping time constant τ	**0.5μs**
Input polarity	**Positive or negative**
Input impedance	**100Ω**
Pole-zero cancellation	**50$\pm$5μs time constant (to match CSPA)**
Gain[1]	**Maximum 50 (20MeV=10V)**
	Minimum 5 (200MeV=10V)
Integral non-linearity	**<0.1%**
Noise	**<1.0mV rms at output (at maximum gain)**
Output	**0-10V into 1kΩ (positive polarity)**
Discriminator	**Leading edge, differentiator time constant 200ns**
Input dynamic range	**0-200MeV (0-2V)**
Threshold[2]	**Adjustable from 10MeV to 0.1MeV**
Time walk	**<20ns over 100:1 dynamic range**
Minimum resolving time	**200ns**
Outputs	**Complementary ECL**
Output width[3]	**Adjustable from 30ns to 200ns**

[1] Gain is adjusted by changing resistors on mother-board
[2] A multi-turn potentiometer on mother-board sets the threshold voltage.
[3] Plug-in resistors on mother-board set pulse width

Table 2: Shaping amplifier and discriminator specification

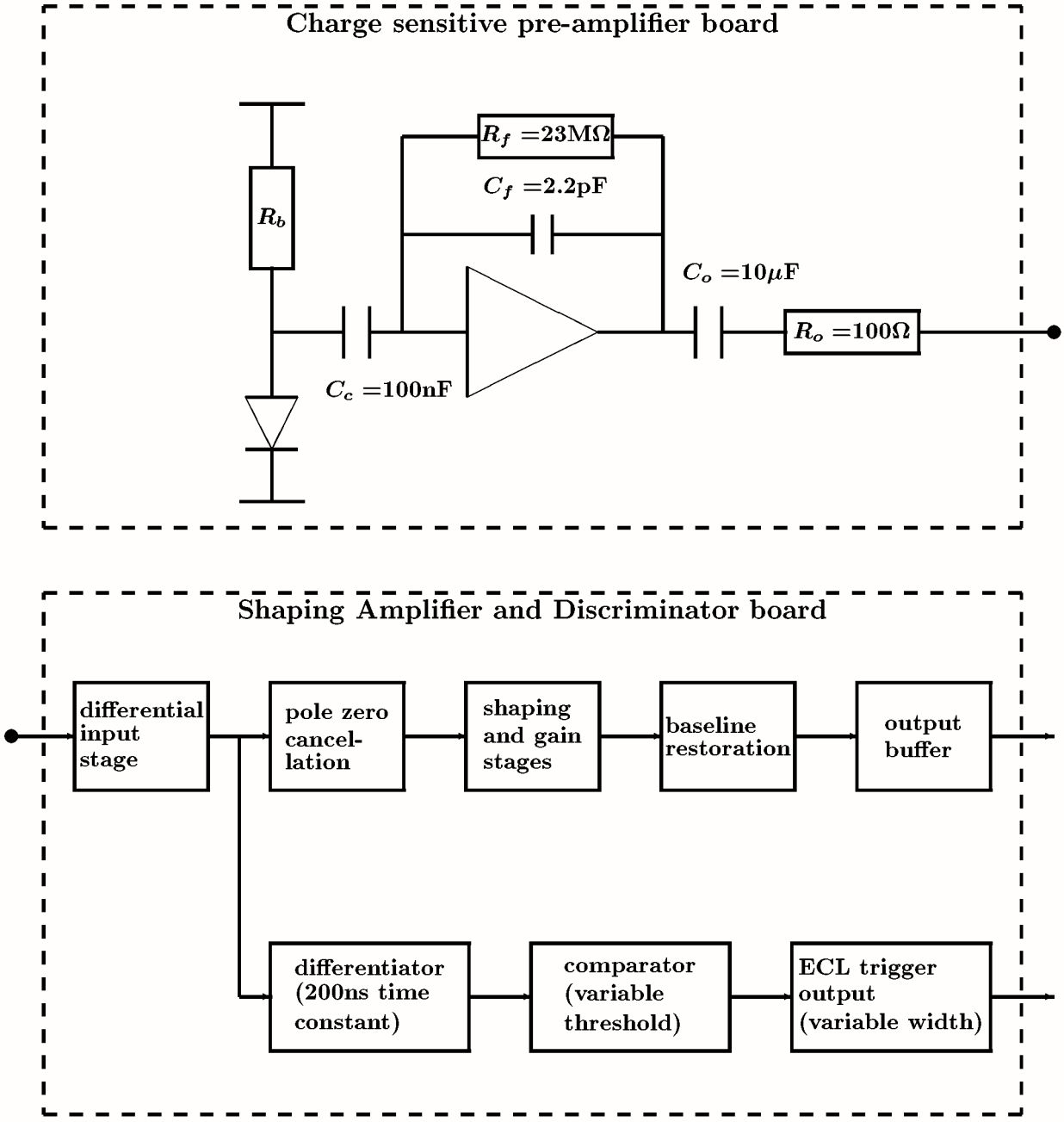

Figure 1: Block diagram of amplifier system

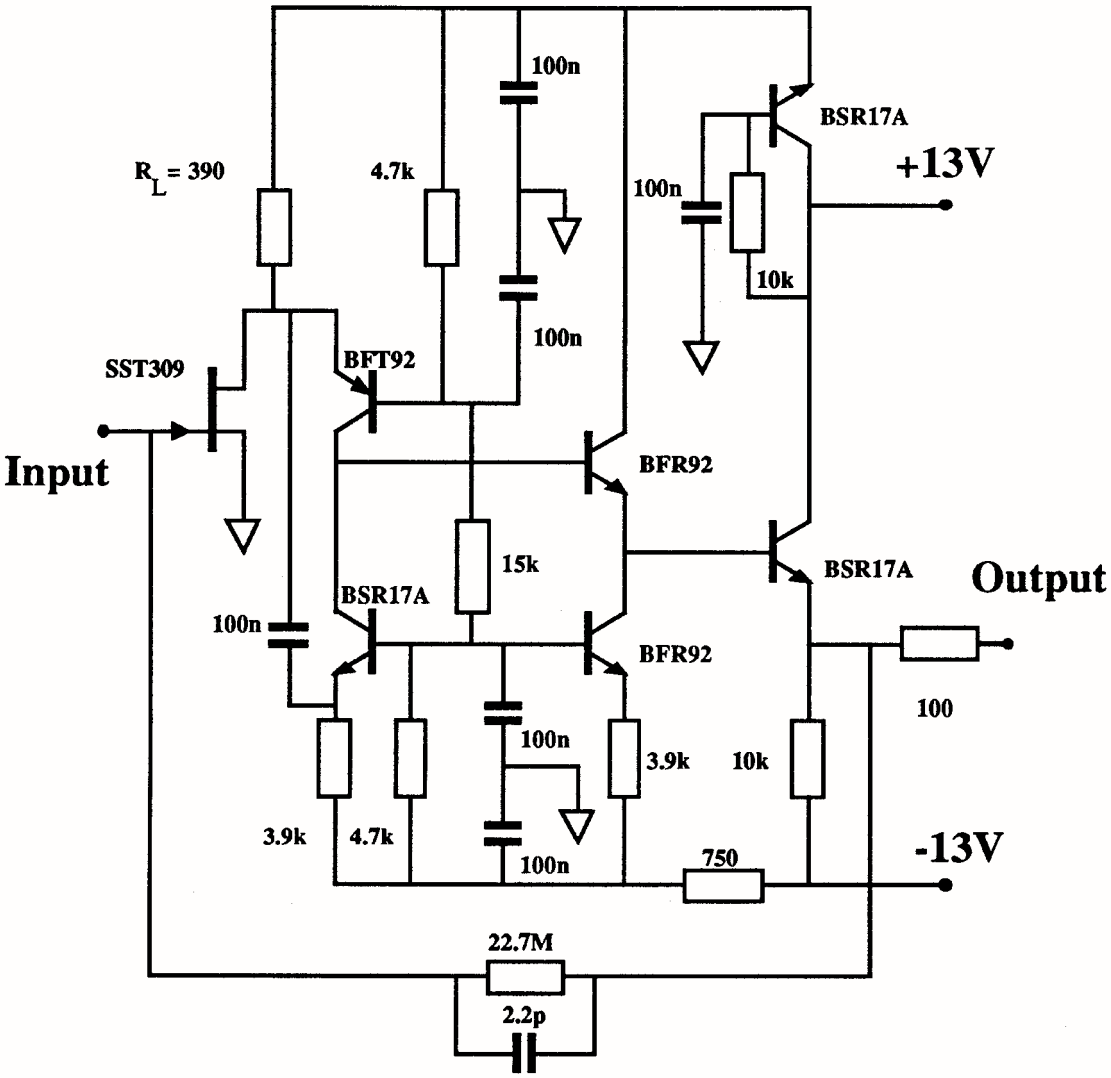

Figure 2a: Charge sensitive pre-amplifier (positive output)

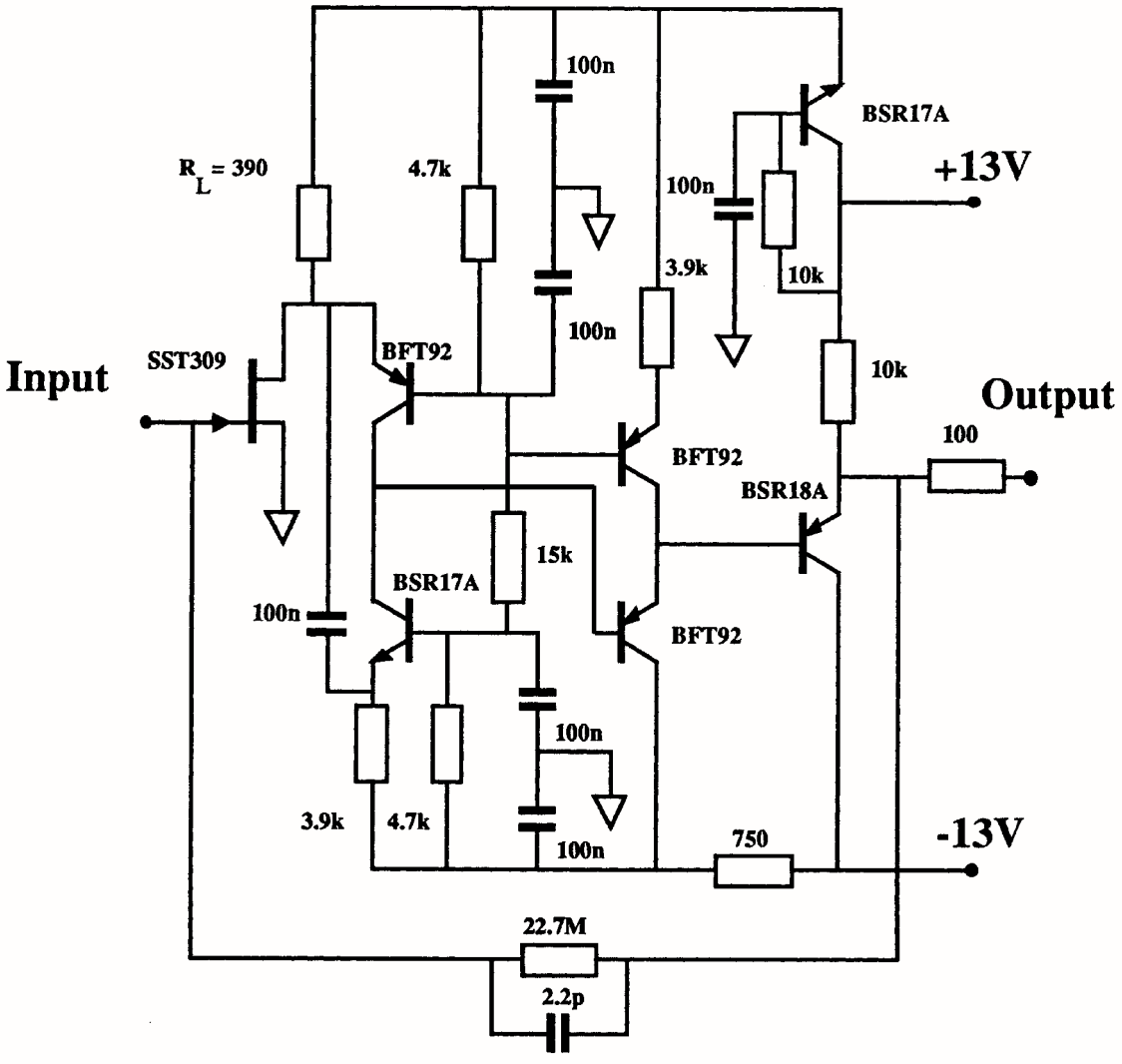

Figure 2b: Charge sensitive pre-amplifier (negative output)

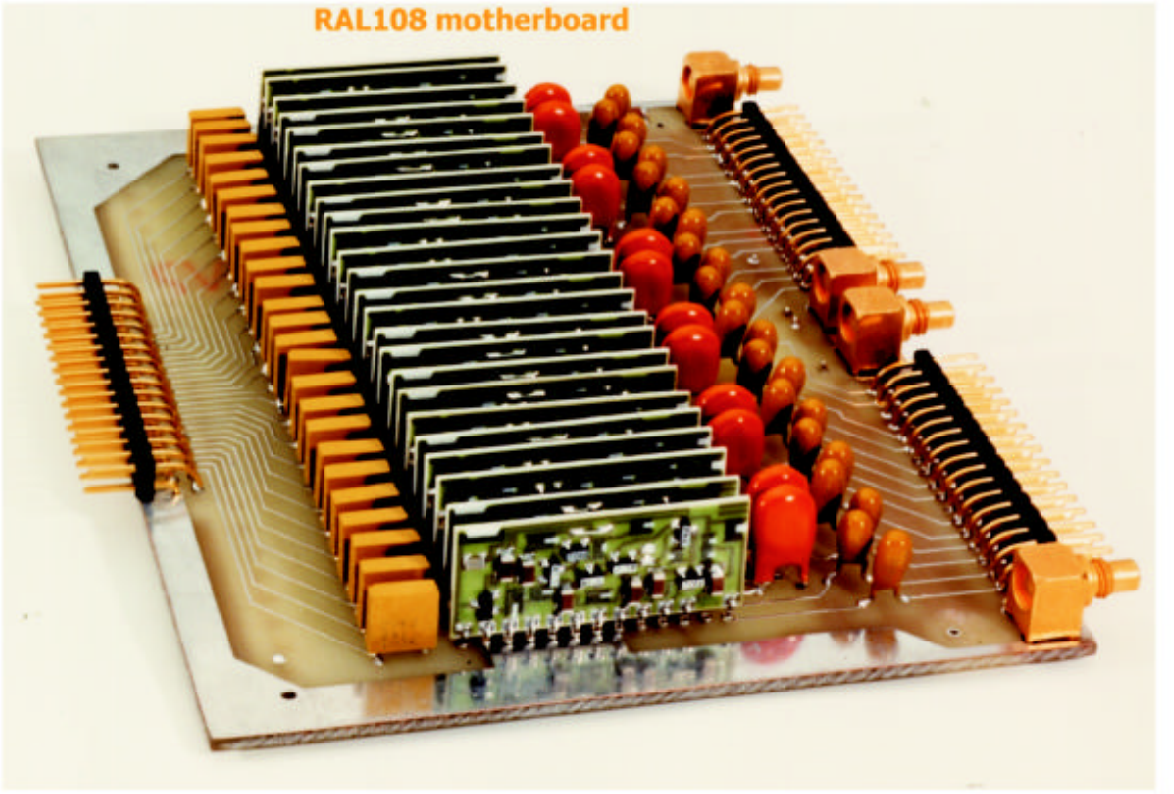

Figure 3: CSPA motherboard (24 channels)

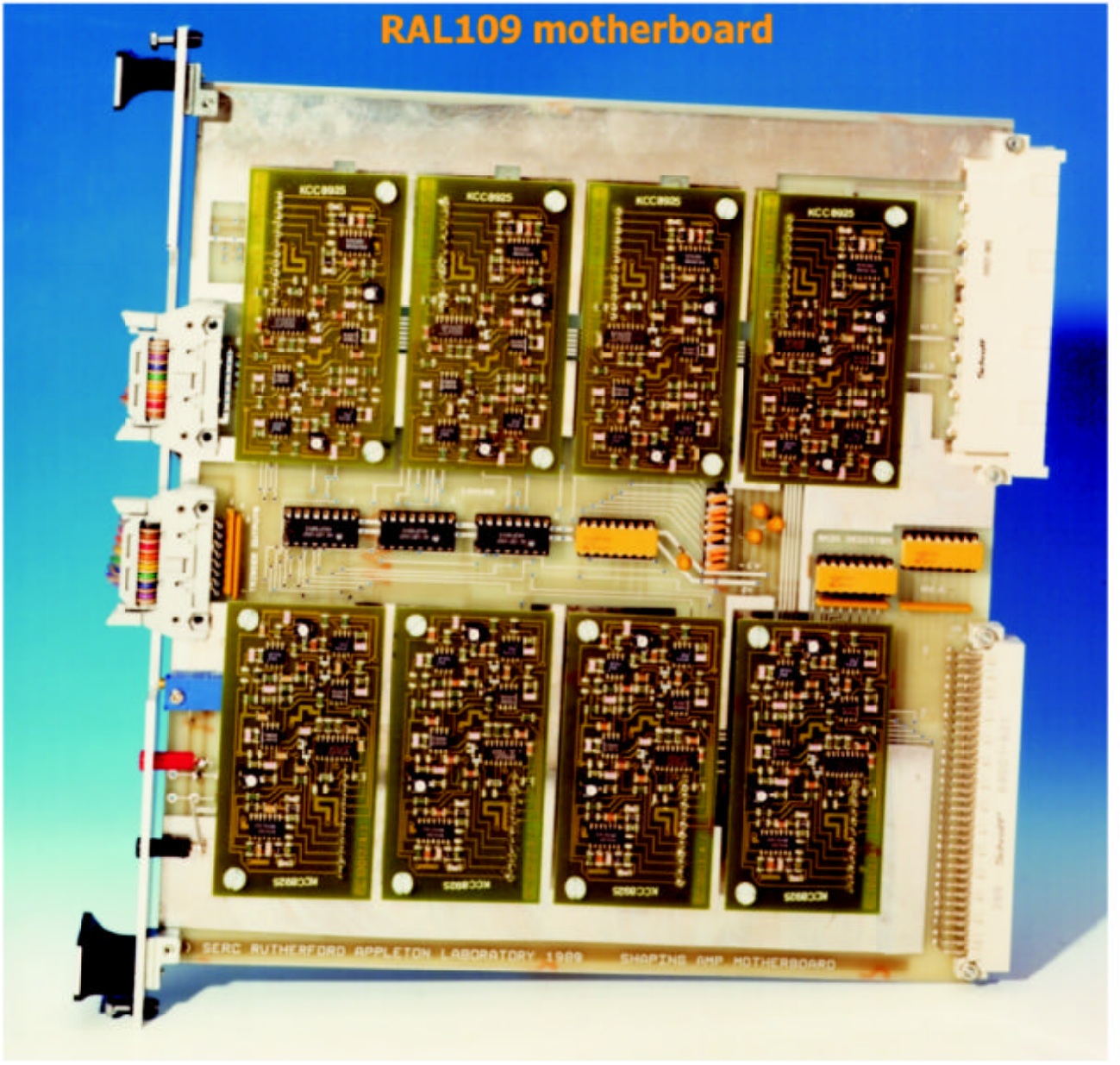

Figure 4: SA motherboard (8 channels)

Notes

1. The two input resistors are in series with DIL plug-ins on the motherboard. Plug-in values in the range 0 - 9 kΩ set the gain of the input buffer.

2. This resistance is an 82kΩ in series with a 50kΩ trimmer which adjusts the pole-zero time constant.

3. The 1kΩ resistors are in a plug-in DIL package. Values from 1kΩ to 2kΩ give output pulse widths from 30 to 200 ns.

4. This resistance is a 2.7kΩ in series with a 5kΩ trimmer which sets the offset of the base-line restorer to zero.

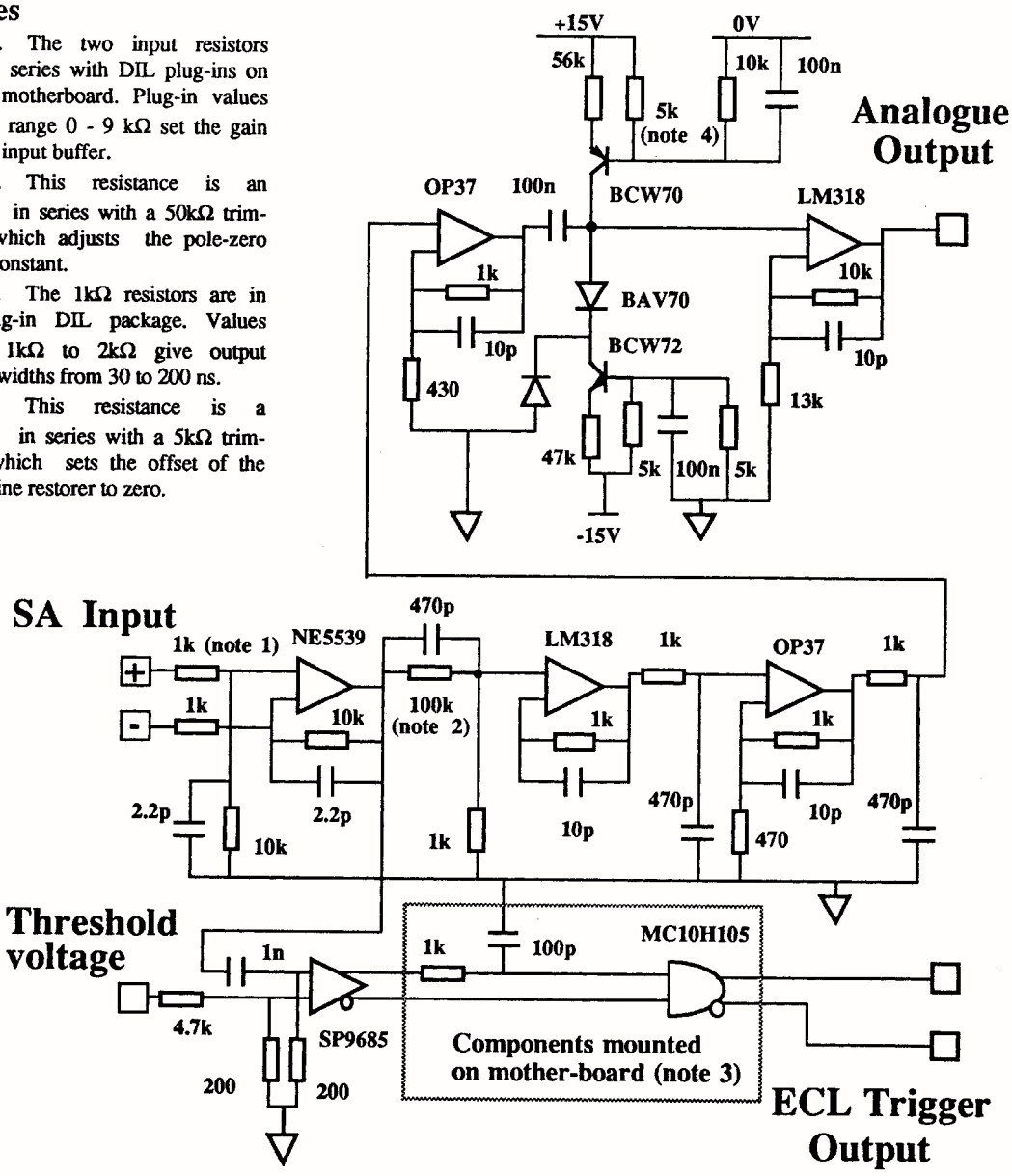

Figure 5: Shaping amplifier and discriminator circuit

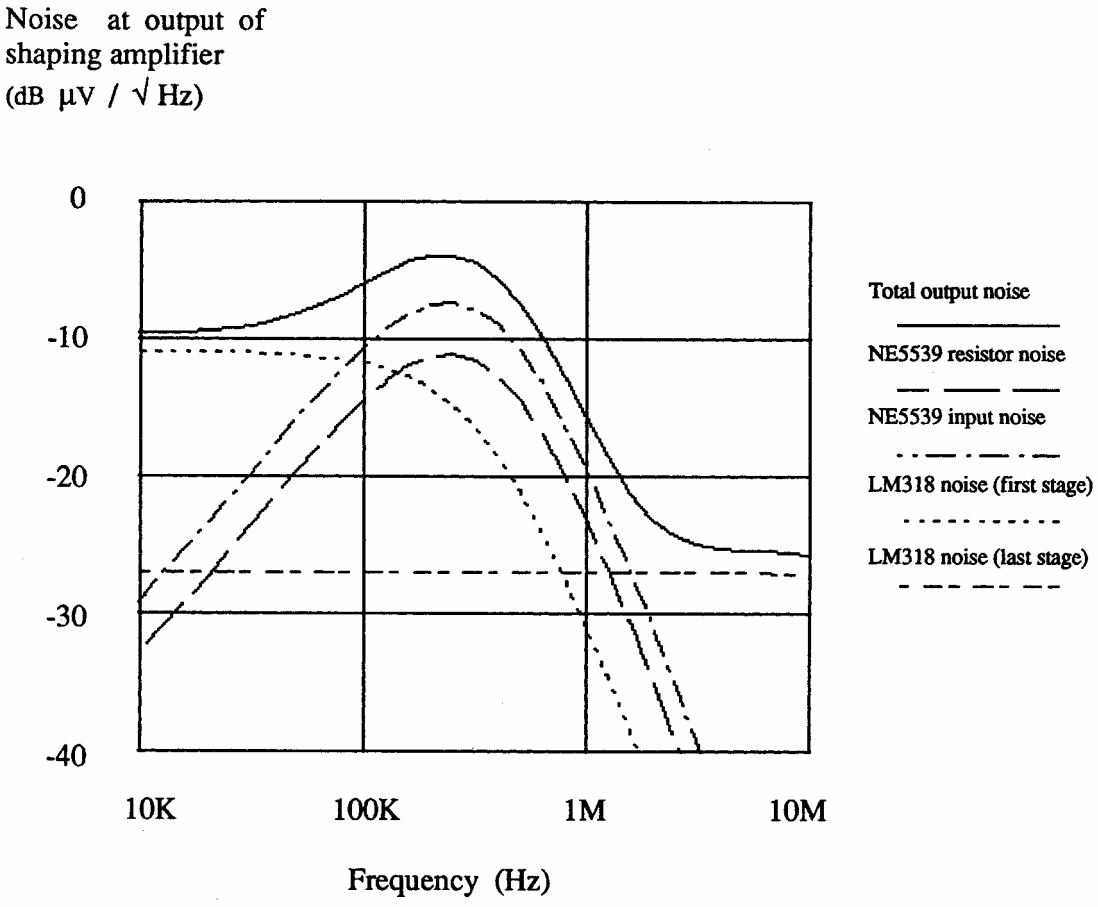

Figure 6: Simulated shaping amplifier noise spectrum

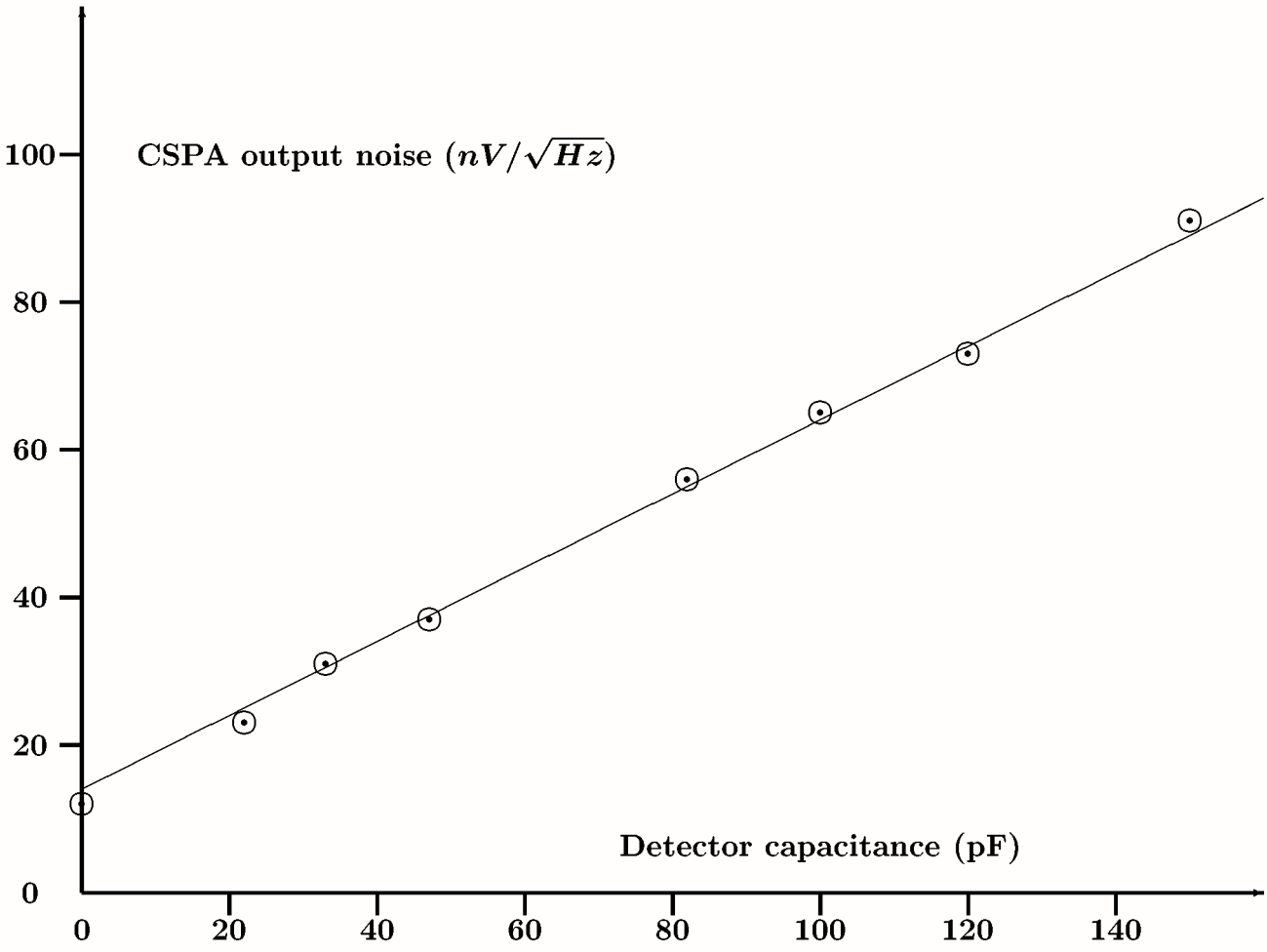

Figure 7: Variation of CSPA output noise density with detector capacitance

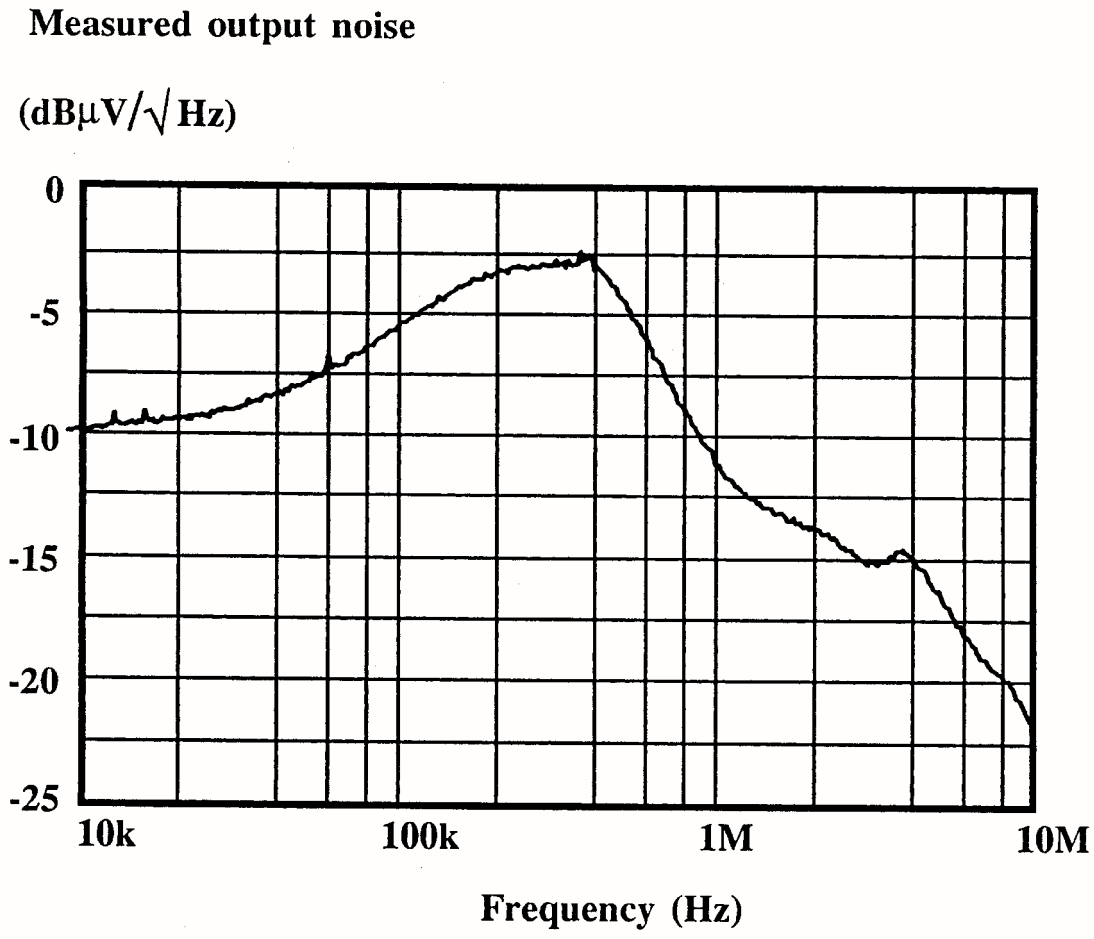

Figure 8: Measured noise spectrum at output of SA